CLAIMS

What is claimed is:

1. An integrated circuit device for receiving a signal transmitted via an electric signal conductor, the integrated circuit device comprising:

a first sampling circuit to sample the signal and generate a first sample value that indicates whether the signal exceeds a first threshold level;

a second sampling circuit to sample the signal and generate a second sample value that indicates whether the signal exceeds a second threshold level; and

a first select circuit coupled to receive the first and second sample values from the first and second sampling circuits and configured to select, according to a previously generated sample value, either the first sample value or the second sample value to be output as a selected sample value.

2. The integrated circuit device of claim 1 further comprising a first storage circuit to store the previously generated sample value, the first storage circuit having an output coupled to a select input of the first select circuit to output the previously generated sample value thereto.

3. The integrated circuit device of claim 2 wherein the first storage circuit has a data input coupled to the first select circuit to receive the selected sample value and a clock input to receive a first clock signal, the first storage circuit being configured to store the selected sample value in response to a transition of the first clock signal.

4. The integrated circuit device of claim 3 wherein the selected sample value, when stored in

the first storage circuit, constitutes the previously generated sample value in relation to a subsequent pair of sample values generated by the first and second sampling circuits.

5. The integrated circuit device of claim 1 wherein the previously generated sample value is generated by one of the first and second sampling circuits prior to generation of the first sample value and the second sample value.

6. The integrated circuit device of claim 1 further comprising:

a third sampling circuit to sample the signal and generate a third sample value that indicates whether the signal exceeds the first threshold level; and

a fourth sampling circuit to sample the signal and generate a fourth sample value that indicates whether the signal exceeds the second threshold level.

7. The integrated circuit device of claim 6 further comprising a second select circuit coupled to receive the third and fourth sample values from the third and fourth sampling circuits, the second select circuit being configured to select either the third sample value or the fourth sample value to be stored in the first storage circuit as the previously generated sample value.

8. The integrated circuit device of claim 7 wherein the first and second sampling circuits are configured to sample the signal in response to a first clock signal, and wherein the third and fourth sampling circuits are configured to sample the signal in response to a second clock signal.

9. The integrated circuit device of claim 8 wherein the second clock signal is phase offset from the first clock signal by a portion of a cycle of the first clock signal such that the third

and fourth sample values are generated at a different time than the first and second sample values.

10. The integrated circuit device of claim 9 wherein the second clock signal is phase offset by a half-cycle of the first clock signal.

11. The integrated circuit device of claim 1 wherein the first sampling circuit comprises a comparator circuit to compare the signal with a first threshold voltage to determine whether the signal exceeds the first threshold level.

12. The integrated circuit device of claim 11 further comprising a threshold generating circuit to generate the first threshold voltage.

13. The integrated circuit device of claim 1 wherein the signal is a differential signal having a first signal component and a second signal component, the second signal component being a complement of the first signal component.

14. The integrated circuit device of claim 13 wherein the first sampling circuit comprises a differential comparator circuit to compare the differential signal against the first threshold level.

15. The integrated circuit device of claim 14 wherein the first threshold level exceeds the common mode of the differential signal.

16. The integrated circuit device of claim 15 wherein the common mode of the differential signal exceeds the second threshold level.

17. The integrated circuit device of claim 16 wherein the common mode of the differential signal is substantially centered between the first and second threshold levels.

18. The integrated circuit device of claim 14 wherein the first threshold level exceeds the common mode of the differential signal by a voltage that corresponds to a level of inter-symbol interference produced by at least one prior signal transmission on the electric signal transmission.

19. The integrated circuit device of claim 1 wherein signal is a multi-level signal representative of more than a single binary bit, and wherein the first sample value generated by the first sampling circuit comprises more than one binary bit.

20. The integrated circuit device of claim 1 further comprising:

a third sampling circuit to compare the signal with a third threshold level and to generate error samples that indicate whether the signal exceeds or is below the third threshold level; and

a threshold generating circuit to adjust the third threshold level until the error samples indicate that the third threshold level substantially matches a first selected level of the signal.

21. The integrated circuit device of claim 20 further comprising a fourth comparator circuit to compare the signal with a fourth threshold level and to generate error samples that indicate whether the signal exceeds or is below the third threshold level, and wherein the threshold generating circuit is configured to adjust the fourth threshold level until the error samples indicate that the fourth threshold level substantially matches a second selected level of the

signal.

22. The integrated circuit device of claim 21 wherein the threshold generating circuit is further configured to generate a first control signal based on the third and fourth threshold levels and to output the first control signal to the first sampling circuit to establish the first threshold level therein.

23. The integrated circuit device of claim 22 wherein the first control signal is a voltage at the first threshold level.

24. The integrated circuit device of claim 22 wherein the first control signal is a digital value representative of the first threshold level.

25. The integrated circuit device of claim 22 wherein the threshold generating circuit is configured to generate the first control signal based on an average of the third and fourth threshold levels.

26. The integrated circuit device of claim 22 wherein the threshold generating circuit is configured to generate the first control signal based on difference between the third and fourth threshold levels.

27. The integrated circuit device of claim 22 wherein the threshold generating circuit is further configured to generate a second control signal based on the third and fourth threshold levels, and to output the second control signal to the second sampling circuit to establish the second threshold level therein

28. The integrated circuit device of claim 22 wherein the threshold generating circuit is further configured to generate a second control value based on the first control value and to output the second control value to the second sampling circuit to establish the second threshold therein.

29. The integrated circuit device of claim 28 wherein threshold generating circuit is configured to generate the second control value by complementing the first control value.

30. A method of operation within an integrated circuit device, the method comprising:
receiving a data signal from an external electrical signaling path;
generating a first data sample having one of at least two states according to whether the data signal exceeds a first threshold level;
generating a second data sample having one of the at least two states according to whether the data signal exceeds a second threshold level; and
selecting either the first data sample or the second data sample to be a selected sample of the data signal.

31. The method of claim 30 wherein selecting either the first data sample or the second data sample to be the selected sample comprises selecting either the first data sample or the second data sample according to whether a third data sample has a first state or a second state.

32. The method of claim 31 further comprising generating the third data sample prior to generating the first and second data samples.

33. The method of claim 30 wherein generating a first data sample comprises generating a first data sample having one of two binary states according to whether the data signal exceeds a first threshold.

34. The method of claim 30 wherein generating a first data sample comprises generating a first data sample having one of more than two possible states.

35. The method of claim 30 wherein the data signal is a differential signal and wherein the first threshold level is above a common mode of the data signal, and the second threshold level is below the common mode of the data signal.

36. The method of claim 35 wherein the common mode of the data signal is substantially centered between the first and second threshold levels.

37. The method of claim 30 further comprising:

determining a first voltage level of the data signal;

determining a second voltage level of the data signal; and

generating the first threshold level based on the first and second voltage levels of the data signal.

38. The method of claim 37 wherein generating the first threshold level based on the first and second voltage levels comprises averaging values representative of the first and second voltage levels to generate a first control value that corresponds to the first threshold level.

39. The method of claim 38 wherein the first control value is a voltage level.

40. The method of claim 38 wherein the first control value is a digital value.

41. The method of claim 37 wherein generating the first threshold level based on the first and second voltage levels comprises subtracting a value representative of the first voltage level from a value representative of the second voltage level to generate a first control value, the first control value corresponding to the first threshold level.

42. An integrated circuit device for receiving a signal transmitted via an electric signal conductor, the integrated circuit device comprising:

a first pair of sampling circuits to capture a first pair of samples of the signal in response to a first clock signal;

a second pair of sampling circuits to capture a second pair of the signal in response to a second clock signal; and

a first select circuit coupled to the first pair of sampling circuits and configured to select one sample of the first pair of samples according to a state of a selected sample of the second pair of samples.

43. The integrated circuit device of 42 further comprising a second select circuit coupled to the second pair of sampling circuits to select the selected sample of the second pair of samples.

44. The integrated circuit device of claim 43 further comprising a first storage circuit coupled to receive the one sample of the first pair of samples from the first select circuit and configured to store the one sample of the first pair of samples in response to the first clock signal.

45. The integrated circuit device of claim 44 wherein an output of the first storage circuit is coupled to a select input of the second select circuit such that the state of a sample stored in the first storage circuit determines which sample of the second pair of samples is selected by the second select circuit.

46. The integrated circuit device of claim 44 further comprising a second storage circuit coupled to receive the selected sample of the second pair of samples from the second select circuit and configured to store the selected sample of the second pair of samples in response to the second clock signal.

47. The integrated circuit device of claim 46 wherein an output of the second storage circuit is coupled to a select input of the first select circuit such that the state of a sample stored in the second storage circuit determines which sample of the first pair of samples is selected by the first select circuit.

48. The integrated circuit device of claim 42 wherein the first clock signal is phase offset from the second clock signal by a portion of a cycle of the second clock signal such that the first pair samples are generated at a different time than the second pair of values.

49. The integrated circuit device of claim 42 wherein the signal is a differential signal and wherein each sampling circuit of the first pair of sampling circuits comprises a differential sampling circuit to generate a respective sample of the first pair of samples.

50. The integrated circuit device of claim 42 wherein a first sampling circuit of the first pair of sampling circuits is configured to determine whether the signal exceeds a first threshold

level, and wherein a second sampling circuit of the first pair of sampling circuits is configured to determine whether the signal exceeds a second threshold level.

51. The integrated circuit device of claim 42 wherein the signal is a differential signal having a first common mode level when at a steady state, and wherein the first common mode level is lower than the first threshold level and above the second threshold level.

52. The integrated circuit device of claim 51 wherein the first common mode level is substantially centered between the first and second threshold levels.

53. A dual mode receive circuit comprising:

compare circuitry to generate first and second samples of an input data signal, each sample having either a first state or a second state according to whether the input data signal exceeds a respective one of first and second threshold levels; and

decision circuitry to generate a received data value based on the first and second samples, the decision circuitry being operable in a first mode to generate a data value having a most significant bit according to the state of the first sample and a least significant bit based, at least in part, on the state of the second sample, the decision circuitry further being operable in a second mode to select either the first sample or the second sample to be the received data value.

54. The dual mode receive circuit of claim 53 wherein the compare circuitry is configured to generate a third sample according to whether the input data signal exceeds a third threshold level.

55. The dual mode receive circuit of claim 54 wherein, in the first mode, the decision circuitry

is configured to generate the least significant bit of the data value according to the states of the second and third samples.

56. The dual mode receive circuit of claim 55 wherein the decision circuitry is configured to generate the least significant bit of the data value in either the first state or the second state according to whether the second and third samples have the same state or different states.

57. The dual mode receive circuit of claim 56 wherein the decision circuitry comprises an exclusive-OR logic circuit to generate the lest significant bit of the data value by exclusive-ORing the second and third samples.

58. The dual mode receive circuit of claim 53 wherein the compare circuitry is configured to generate the first and second samples of the input data signal in response to a transition of a first clock signal.

59. The dual mode receive circuit of claim 53 further comprising a configuration control circuit to store a mode select value, the dual mode receive circuit being responsive to the mode select value to operate in either the first mode or the second mode.

60. The dual mode receive circuit of claim 53 further comprising a threshold generating circuit, the threshold generating circuit being configured to determine first and second signal levels of the input data signal and to generate the first and second threshold levels based on the first and second signal levels.

61. The dual mode receive circuit of claim 53 wherein, when the dual mode circuit is operated in the first mode, the first and second signal levels of the input signal are indicative of a

signal swing of the input data signal, and wherein the threshold generating circuit is further configured to establish the first threshold level at a first voltage level substantially centered within the signal swing.

62. The dual mode receive circuit of claim 61 wherein the threshold generating circuit is further configured to establish the second threshold level at a second voltage level substantially centered between the first voltage level and a first peak level of the signal swing.

63. The dual mode receive circuit of claim 62 wherein the first peak level of the signal swing is an upper peak of the signal swing and wherein the threshold generating circuit is further configured to generate a third threshold level that is substantially centered between the first voltage level and a lower peak level of the signal swing.

64. The dual mode receive circuit of claim 53 wherein, in the second mode, the decision circuitry is operable to select either the first sample or second sample according to whether a third sample is in the first state or the second state, the third sample being generated prior to the first and second samples.

65. The dual mode receive circuit of claim 64 wherein the decision circuitry comprises a select circuit having first and second inputs to receive the first and second samples, respectively, and a select input coupled to receive the third sample, the select circuit being configured to output either the first sample or the second sample as the received data value according to the state of the third sample.

66. The dual mode receive circuit of claim 65 further comprising a storage circuit coupled to

receive the received data value from the select circuit, the received data value constituting the third sample in relation to subsequent instances of the first and second samples generated by the compare circuitry.

67. The dual mode receive circuit of claim 53 further comprising a threshold generating circuit, the threshold generating circuit being configured to generate the first and second thresholds at a first pair of voltage levels when the dual mode circuit is operated in the first mode, and to generate the first and second thresholds at a second pair of voltage levels when the dual mode circuit is operated in the second mode.

68. The dual mode receive circuit of claim 67 wherein the first pair of voltages are generated according to a signal swing of the input data signal.

69. The dual mode receive circuit of claim 68 wherein the threshold generating circuit comprises a level sampling circuit to determine the signal swing of the input data signal.

70. The dual mode receive circuit of claim 69 wherein the level sampling circuit is configured to determine a first voltage level of the input data signal that corresponds to a first symbol value, and a second voltage level of the input data signal that corresponds to a second symbol value, the signal swing of the input data signal being determined based on the first and second voltage levels.

71. The dual mode receive circuit of claim 68 wherein the second pair of voltages are generated according to a level of inter-symbol interference detected in the input data signal.

72. A method of operation within an integrated circuit device, the method comprising:

generating first and second samples of an input data signal, each sample having either a first state or a second state according to whether the input data signal exceeds a respective one of first and second threshold levels;

generating a first received data value based on the first and second data samples if a mode select signal is in a first state; and

generating a second received data value based on the first and second data samples if the mode select signal is in a second state, wherein the second received data value includes more constituent bits than the first received data value.

73. The method of claim 72 wherein the second received data value comprises at least two constituent bits.

74. The method of claim 73 wherein the first received data value comprises one bit.

75. The method of claim 72 wherein generating the second received data value comprises:

generating a most significant bit of the second received data value according to the state of the first sample; and

generating a least significant bit of the second received data value based, at least in part, on the state of the second sample.

76. The method of claim 72 further comprising generating a third sample having either the first state or the second state according to whether the input data signal exceeds a third threshold level.

77. The method of claim 76 wherein generating the second received data value comprises:

generating a most significant bit of the second received data value according to the state of

the first sample; and

generating a least significant bit of the second received data value according to the states of the second and third samples.

78. The method of claim 77 wherein generating the least significant bit comprises generating the least significant bit in either the first state or the second state according to whether the second and third samples have the same state or different states.

79. The method of claim 77 wherein generating the least significant bit comprises generating an exclusive-OR combination of the second and third samples.

80. The method of claim 72 wherein generating first and second samples of an input data signal comprises sampling the input data signal in response to a transition of a first sample control signal.

81. The method of claim 80 wherein the first sample control signal is a clock signal.

82. The method of claim 72 wherein generating the first received data value comprises selecting either the first sample or the second sample to be the received data value.

83. The method of claim 82 wherein selecting either the first sample or the second sample to be the received data value comprises selecting either the first sample or the second sample according to whether a third sample is in the first state or the second state.

84. The method of claim 83 further comprising generating the third sample prior to generating the first and second samples.

85. The method of claim 72 further comprising generating the first and second threshold levels.

86. The method of claim 85 wherein generating the first and second threshold levels comprises generating a first pair of threshold levels when the mode select signal is in the first state, and generating a second pair of threshold levels when the mode select signal is in the second state.

87. The method of claim 86 wherein generating the first pair of threshold levels comprises generating the first pair of threshold levels based on a signal swing of the input signal.

88. The method of claim 86 wherein generating the second pair of threshold levels comprises generating the second pair of threshold levels based on a level of inter-symbol interference in the input data signal.

89. A clock data recovery circuit comprising:

a data sampling circuit to generate data samples of an input data signal in response to a first clock signal;

an edge sampling circuit to generate edge samples of the input data signal in response to a second clock signal; and

a clock recovery circuit coupled to receive the edge samples and the data samples, the clock recovery circuit being configured to adjust a phase of the second clock signal according to the state of one of the edge samples upon determining that a sequence of at least three of the data samples matches at least one sample pattern of a plurality of predetermined sample patterns.

90. The clock data recovery circuit of claim 89 wherein the clock recovery circuit comprises a clock generating circuit to generate the first and second clock signals.

91. The clock data recovery circuit of claim 89 wherein the sequence of at least three of the data samples comprises two data samples generated prior to the one of the edge samples, and one data sample generated after the one of the edge samples.

92. The clock data recovery circuit of claim 91 wherein the sequence of at least three of the data samples comprises first, middle and last samples, and wherein the sequence of at least three of the data samples is determined to match the at least one sample pattern if (1) the first and last samples have the same state and (2) at least one of the first and last samples has a different state than the middle sample.

93. The clock data recovery circuit of claim 89 wherein the edge sampling circuit comprises a first compare circuit to compare the input data signal with a first threshold level and to generate a first subset of the edge samples in response to the second clock signal, each edge sample of the first subset having either a first state or a second state according to whether the input data signal exceeds the first threshold level.

94. The clock data recovery circuit of claim 93 wherein the first threshold level is substantially centered between steady-state high and low levels of the input data signal.

95. The clock data recovery circuit of claim 93 wherein the edge sampling circuit further comprises a second compare circuit to compare the input data signal with a second threshold level and to generate a second subset of the edge samples in response to the

second cock signal, each edge sample of the second subset having either the first state or the second state according to whether the input data signal exceeds the second threshold.

96. The clock data recovery circuit of claim 95 wherein the one of the edge samples is selected from either the first subset of the edge samples or the second subset of the edge samples according to whether the sequence of at least three of the data samples matches a first sample pattern of the plurality of predetermined sample patterns or a second sample pattern of the predetermined sample patterns.

97. The clock data recovery circuit of claim 95 wherein the edge sampling circuit further comprises a third compare circuit to compare the input data signal with a third threshold level and to generate a third subset of the edge samples in response to the second cock signal, each edge sample of the third subset having either the first state or the second state according to whether the input data signal exceeds the third threshold.

98. The clock data recovery circuit of claim 97 wherein the one of the edge samples is selected from either the first second or third subset of the edge samples according to whether the sequence of at least three of the data samples matches a first sample pattern, second sample pattern or third sample pattern, respectively, of the plurality of predetermined sample patterns.

99. The clock data recovery circuit of claim 98 wherein the first threshold level is substantially centered between the second and third threshold levels.

100. The clock data recovery circuit of claim 98 wherein the first sample pattern comprises two successive data state transitions in the at least three of the data samples.

101. The clock data recovery circuit of claim 98 wherein the second sample pattern comprises two same-state data samples followed by a data sample having a different state than the same-state data samples.

102. The clock data recovery circuit of claim 101 wherein the two same-state data samples are logic ‘0’ values.

103. The clock data recovery circuit of claim 102 wherein the third sample pattern comprises two logic ‘1’ data samples followed by a logic ‘0’ data sample.

104. The clock data recovery circuit of claim 89 wherein transitions of the second clock signal are substantially phase aligned with transitions in the input data signal.

105. The clock data recovery circuit of claim 104 wherein transitions of the first clock signal are substantially centered within data valid intervals of the input data signal.

106. An integrated circuit device comprising:

a first sampling circuit to sample an input data signal at a time that corresponds to a transition interval within the input data signal, the first sampling circuit being configured to generate a sample value having either a first state or a second state according to whether the input data signal, when sampled, is above or below a selected threshold level; and

a threshold generating circuit to establish the selected threshold level within the first sampling circuit, the threshold generating circuit establishing the selected threshold level at a first threshold level if a mode select signal is in a first state, and establishing

the selected threshold at a second threshold level if the mode select signal is in a second state.

107. The integrated circuit device of claim 106 wherein the first state of the mode select signal corresponds to a binary signal reception mode within the integrated circuit device, and wherein the second state of the mode select signal corresponds to a multi-level signal reception mode within the integrated circuit device.

108. The integrated circuit device of claim 106 further comprising a clock recovery circuit to generate a first clock signal that transitions at the time that corresponds to the transition interval within the input data signal.

109. The integrated circuit device of claim 108 wherein the clock recovery circuit is coupled to receive the sample value generated by the first sampling circuit and is configured to advance or retard the phase of the first clock signal based, at least in part, on the state of the sample value.

110. A clock data recovery circuit comprising:

a data sampling circuit to capture a first sample of a data signal at a first time and a second sample of the data signal at a second time, each of the first and second samples corresponding to a respective one of at least three possible signal levels of the data signal;

an edge sampling circuit to capture a third sample of the data signal at an intervening time between the first and second time; and

a clock recovery circuit coupled to receive the first and second samples from the data

sampling circuit and the third sample from the edge sampling circuit, the clock recovery circuit being configured to adjust a phase of a first clock signal according to the third sample if the first sample and second sample indicate a transition in the data signal that is one of a predetermined subset of possible transitions between the at least three possible signal levels.

111. The clock data recovery circuit of claim 110 wherein each of the first and second samples comprises at least two binary bits and corresponds to a respective one of at least four possible signal levels.

112. The clock data recovery circuit of claim 111 wherein the data sampling circuit comprises:
a first compare circuit to compare the data signal with a first threshold level and to generate a first bit of the at least two binary bits in either a first state or a second state according to whether the data signal exceeds the first threshold level; and
a second compare circuit to compare the data signal with a second threshold level and to generate a second bit of the at least two binary bits in either the first state or the second state according to whether the data signal exceeds the second threshold level.

113. The clock data recovery circuit of claim 112 further comprising a threshold generating circuit to determine a level of inter-symbol interference present in the data signal and to generate the first and second threshold levels according to the level of inter-symbol interference.

114. The clock data recovery circuit of claim 111 wherein the at least two binary bits comprise a most significant bit and a least significant bit.

115. The clock data recovery circuit of claim 114 wherein the data sampling circuit comprises: a first compare circuit to compare the data signal with a first threshold level and to generate the most significant bit in either a first state or a second state according to whether the data signal exceeds the first threshold level; a second compare circuit to compare the data signal with a second threshold level to generate a first intermediate result; a third compare circuit to compare the data signal with a third threshold level to generate a second intermediate result; and a logic circuit coupled to the second and third compare circuits and configured to generate the least significant bit in either the first state or the second state according to the first and second intermediate results.

116. The clock data recovery circuit of claim 115 wherein the logic circuit is configured to generate the least significant bit in the first state if the first intermediate result matches the second intermediate result, and in the second state if the first intermediate result does not match the second intermediate result.

117. The clock data recovery circuit of claim 115 wherein the logic circuit is an exclusive OR gate.

118. The clock data recovery circuit of claim 115 wherein the first threshold level is substantially centered between the second and third threshold levels.

119. A method of recovering a clock signal from a data signal, the method comprising generating a first sample of the data signal at a first time and a second sample of the data

signal at a second time, each of the first and second samples corresponding to a respective one of at least three possible signal levels of the data signal;

generating a third sample of the data signal at an intervening time between the first time and the second time; and

adjusting a phase of a first clock signal according to the third sample if the first sample and the second sample indicate a transition in the data signal that is one of a predetermined subset of possible transitions between the at least three possible signal levels.

120. The method of claim 119 wherein each of the first and second samples of the data signal comprises at least two binary bits and corresponds to a respective one of at least four possible signal levels.

121. The method of claim 120 wherein generating the first sample value comprises comparing the data signal with a first threshold level to generate a first one of the binary bits and comparing the data signal with a second threshold level to generate a second one of the binary bits.

122. The method of claim 121 further comprising generating the first and second threshold levels according to a level of inter-symbol interference present in the data signal.

123. The method of claim 120 wherein the at least two binary bits comprise a most significant bit and a least significant bit.

124. The method of claim 123 wherein generating the first sample value comprises comparing the data signal with a first threshold level to determine the state of the most significant bit,

and determining the data signal with second and third threshold levels to determine the state of the least significant bit.

125. The method of claim 124 wherein the first threshold level is substantially centered between the second and third threshold levels.

126. The method of claim 119 further comprising determining whether the first and second samples indicate a transition in the data signal that is one of the predetermined subset of the possible transitions between the at least three possible signal levels.

127. The method of claim 126 wherein the predetermined subset of the possible transitions between the at least three possible signal levels comprises transitions that ideally cross a first threshold level at a time substantially centered between the first time and the second time.

128. The method of claim 127 wherein the predetermined subset of the possible transitions between the at least three possible signal levels further comprises transitions that ideally cross a second threshold level at a time substantially centered between the first time and the second time.

129. The method of claim 128 wherein the predetermined subset of the possible transitions between the at least three possible signal levels further comprises transitions that ideally cross a third threshold level at a time substantially centered between the first time and the second time.

130. The method of claim 129 wherein the first threshold level is substantially centered between

the second threshold level and the third threshold level.

131. The method of claim 130 wherein the first data sample comprises first and second binary bits, and wherein generating the first data sample comprises comparing the data signal with the first threshold level to generate the first binary bit, and comparing the data signal with the second threshold level and the third threshold level to generate the second binary bit.

132. The method of claim 119 wherein the predetermined subset of possible transitions between the at least three possible signal levels is indicated by a configuration value.

133. The method of claim 132 further comprising storing the configuration value within a configuration circuit.

134. The method of claim 119 wherein generating the first sample of the data signal at the first time comprises generating the first sample of the data signal in response to a first transition of a second clock signal.

135. The method of claim 134 wherein generating the second sample of the data signal at the second time comprises generating the second sample of the data signal in response to a second transition of the second clock signal.

136. The method of claim 135 wherein the first transition of the second clock signal is a rising edge transition and wherein the second transition of the second clock signal is a falling edge transition.

137. The method of claim 134 wherein generating the second sample of the data signal at the

second time comprises generating the second sample of the data signal in response to a transition of a third clock signal that is phase shifted relative to the second clock signal by a portion of a cycle of the second clock signal.

138. The method of claim 134 wherein generating the second sample of the data signal at the second time comprises generating the second sample of the data signal in response to a transition of a third clock signal that is a complement of the second clock signal.

139. The method of claim 134 wherein generating the third sample at the intervening time comprises generating the third sample in response to a transition of a first clock signal, the first clock cycle being phase offset from the second clock cycle by a portion of a cycle of the second clock signal.

140. The method of claim 139 wherein adjusting the phase of the first clock signal comprises advancing or retarding the phase of the first clock signal according to whether the third sample is in a first state or a second state.

141. The method of claim 139 wherein adjusting the phase of the first clock signal comprises advancing or retarding the phase of the first clock signal according to whether the third sample indicates that the transition in the third clock signal lags or leads the transition in the data signal.

142. A method of operation within a signaling system, the method comprising:

outputting a sequence of data values onto an electric signal conductor during successive transmission intervals, the sequence of data values forming a data signal on the electric signal conductor;

generating, during each of a sequence of data reception intervals, a first data sample having either a first state or second state according to whether a signal level of the electric signal conductor exceeds a first threshold level and a second data sample having either the first state or second state according to whether the signal level exceeds a second threshold level; and

selecting, during each of the data reception intervals after a first one of the data reception intervals, either the first data sample or the second data sample to be a received data value according to the state of at least one received data value selected during a prior reception interval.

143. The method of claim 142 wherein selecting either the first data sample or the second data sample to be the received data value comprises selecting either the first data sample or the second data sample to be the received data value according to the state of a received data value selected during an immediately preceding one of the reception intervals.

144. The method of claim 142 wherein selecting either the first data sample or the second data sample to be the received data value according to the state of the at least one received data value comprises selecting, during one of the data reception intervals, either the first data sample or the second data sample to be the received data value according to the state of N received data values selected during N respective reception intervals that precede the one of the data reception intervals, N being an integer value greater than zero.

145. The method of claim 144 wherein outputting the sequence of data values comprises outputting an equalizing signal onto the electric signal conductor during each one of the transmission intervals to reduce inter-symbol interference resulting from data values

transmitted more than N transmission intervals prior to the one of the transmission intervals.

146. The method of claim 145 wherein outputting an equalizing signal onto the electric signal conductor comprises generating an equalizing signal according to at least one of the data values transmitted more than N transmission intervals prior to the one of the transmission intervals.

147. The method of claim 146 wherein generating the equalizing signal further comprises generating the equalization signal in an output driver in accordance with a weighting value that controls a signal drive strength of the output driver.

148. A signal receiving circuit comprising:

first and second output lines coupled to a reference voltage via first and second resistive elements, respectively;

a first differential amplifier coupled to the first and second output lines and configured to draw first and second currents through the first and second resistive elements in accordance with respective signal levels of an input signal and complement input signal;

a second differential amplifier coupled to the first and second output lines and configured to draw third and fourth currents through the first and second resistive elements in accordance with respective signal levels of an input signal and complement input signal; and

a sampling circuit coupled to the first and second output lines and configured to store a sampled data value having either a first state or a second state according to respective

voltage levels generated on the first and second output lines by the first, second, third and fourth currents.

149. The signal receiving circuit of claim 148 wherein the first differential amplifier comprises first and second transistors having respective control terminals coupled to receive the input signal and complement input signal.

150. The signal receiving circuit of claim 149 wherein the first and second transistors have respective output terminals coupled to the first and second output lines, and respective reference terminals coupled to one another.

151. The signal receiving circuit of claim 150 further comprising a first current source coupled to the reference terminals of the first and second transistors.

152. The signal receiving circuit of claim 148 wherein the voltage level generated on the first output line is established by a voltage drop across the first resistive element due to the first current and the third current, and wherein the voltage level generated on the second output line is established by a voltage drop across the second resistive element due to the second current and the fourth current.

153. The signal receiving circuit of claim 148 wherein the first differential amplifier comprises a first transistor to draw the first current according to the signal level of the input signal, and a second transistor to draw the second current according to the signal level of the complement input signal, and wherein the gain of the first transistor is greater than the gain of the second transistor such that, when the signal levels of the input signal and complement input signal are equal, the first current is greater than the second current.

154. The signal receiving circuit of claim 153 wherein the first transistor is wider than the second transistor to achieve the greater gain.

155. The signal receiving circuit of claim 153 wherein the second differential amplifier comprises a third transistor to draw the third current according to the signal level of the input signal, and a fourth transistor to draw the fourth current according to the signal level of the complement input signal, and wherein the gain of the fourth transistor is greater than the gain of the third transistor such that, when the signal levels of the input signal and complement input signal are equal, the fourth current is greater than the third current.

156. The signal receiving circuit of claim 155 wherein the gain of the fourth transistor is substantially the same as the gain of the first transistor, and the gain of the second transistor is substantially the same as the gain of the third transistor.

157. The signal receiving circuit of claim 148 further comprising a first adjustable current source coupled to the first differential amplifier, and a second adjustable current source coupled to the second differential amplifier.

158. The signal receiving circuit of claim 157 wherein the first adjustable current source is configured to draw a first bias current in accordance with a first control value, and wherein a sum of the first and second currents drawn by the first differential amplifier is substantially equal to the first bias current.

159. The signal receiving circuit of claim 158 wherein the second adjustable current source is configured to draw a second bias current in accordance with a second control value, and

wherein a sum of the third and fourth currents drawn by the second differential amplifier is substantially equal to the second bias current.

160. The signal receiving circuit of claim 157 wherein the first adjustable current source comprises a plurality of biasing transistors coupled in parallel between the first differential amplifier and a reference voltage, each of the biasing transistors having a control terminal coupled to receive a respective bit of a control value.

161. The signal receiving circuit of claim 160 wherein each of the biasing transistors is configured to conduct a respective biasing current when the respective bit of the control value is in a first state and to switch to a substantially non-conducting condition when the respective bit of the control value is in a second state.

162. The signal receiving circuit of claim 160 wherein at least one of the biasing transistors has a different gain than another of the biasing transistors.

163. The signal receiving circuit of claim 148 wherein at least one of the first and second resistive elements includes a transistor.

164. A method of operation within an integrated circuit device, the method comprising:

generating first and second currents in a first differential amplifier in accordance with signal levels of an input signal and complement input signal, respectively, the first current flowing through a first resistive element coupled between a supply voltage and a first output line, and the second current flowing through a second resistive element coupled between the supply voltage and a second output line;

generating third and fourth currents in a second differential amplifier in accordance with

signal levels of the input signal and complement input signal, respectively, the third current flowing through the first resistive element, and the fourth current flowing through the second resistive element; and

storing a sampled data value having either a first state or a second state according to respective voltage levels generated on the first and second output lines by the first, second, third and fourth currents.

165. The method of claim 164 wherein the respective voltage levels generated on the first and second output lines comprise a first voltage level generated on the first output line by a voltage drop across the first resistive element.

166. The method of claim 165 wherein the voltage drop across the first resistive element is generated by first and second currents flowing through the first resistive element.

167. The method of claim 164 wherein generating the first and second currents in the first differential amplifier comprises generating unequal current levels for the first current and the second current when the input signal and complement signal are equal.

168. The method of claim 167 wherein generating the third and fourth currents in the second differential amplifier comprises generating unequal current levels for the third current and the fourth current when the input signal and complement signal are equal.

169. The method of claim 168 wherein the first current and the fourth current are substantially equal when the input signal and complement signal are equal, and wherein the second current and the third current are substantially equal when the input signal and complement input signal are equal.

170. The method of claim 169 wherein the first current exceeds the second current when the input signal and complement signal are equal.

171. The method of claim 164 further comprising generating a first bias current in response to a first control value and generating a second bias current in response to a second control value, wherein the first and second currents sum to a total current determined by the first bias current, and wherein the third and fourth currents sum to a total current determined by the second bias current.